ABSTRACT

A method and architecture for improving the usability and manufacturing yield of a microprocessor having a large on-chip n-way set associative cache. The architecture provides a method for working around defects in the portion of the die allocated to the data array of the cache. In particular, by adding a plurality of muxes to a way or ways in the data array of an associative cache having the shorter paths to the access control logic, each way in a bank can be selectively replaced or remapped to the ways with the shorter paths without adding any latency to the system. This selective remapping of separate ways in individual banks of the set associative cache provides a more efficient way to absorb defects and allows more defects to be absorbed in the data array of a set associative cache.